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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,374	04/20/2004	Lawrence A. Clevenger	YOR920010247DIV	4885

29154 7590 04/11/2006

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EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,374	CLEVENGER ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-20* is/are allowed.

6)☒ Claim(s) *11-15 & 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 3/21/2006 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, regarding claims 11-15 the applicant contends the "conductive polymer bumps do not comprise passive devices". The examiner would like to point out that the conductive polymer bumps are the passive devices. A passive device in any device incapable of current gain or switching. A conductive polymer bumps are electrical contacts, which are merely short conductive wires. A conductive wire is a passive device, therefore interently a conductive polymer bump is a passive device. The purpose of the using Murphy in combination with Higgins is merely to show that it is obvious that if one skilled in the art can print a conductive polymer on a substrate it is very obvious they could also print the conductive polymer on an IC, wherein the polymer is obviously printed on the "exterior conductor level" (Higgins, Fig. 4). Therefore the arguments directed to claims 11-15 are not persuasive and are considered moot.

DETAILED ACTION

Allowable Subject Matter

Claims 16-20 are allowed. The following is an examiner's statement of reasons for allowance: Murphy et al. teaches the method of forming conductive polymer passive devices on a substrate, in which it would be obvious to one of ordinary skill in the art from the devices on a preformed wiring / IC substrate. From the prior art it would not however be obvious to one of ordinary skill in the art to form the passive devices on a substrate and then transfer the individual passive devices to the IC as claimed in claim 16. Claims 17-20 are dependent upon claim 16 therefore they are allowable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al. (US 5,855,755) in view of Higgings, III (US 5,492,863)

Regarding claim 11, Murphy teaches a method of manufacturing an integrated circuit chip structure comprising:

supplying an integrated circuit chip; and

patterning a conductive polymer directly on an exterior conductor level of said integrated circuit chip, wherein said patterning produces passive devices.

(Murphy, Col. 4, lines 10-15)

Murphy et al. teaches that the patterned passive devices are formed on the surface of a substrate. It is generally understood in the art, that an integrated circuit can be preformed on or in the substrate or produced after passive devices are formed. However, Murphy et al. does not explicitly teach that the conductive polymer film is formed on a supplied integrated circuit chip.

Higgins teaches the method in which an IC chip is provided (Higgins, Fig. 1 – IC Figs. 2-4 show patterning of conductive polymer layer 18). (Higgins, claims 1 & 14)

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to pattern a conductive polymer layer on a provided IC chip.

The application of the conductive polymer to the wafer and the subsequent lithographic processing involves straight forward processing technologies, without need for knowledge of the elaborate techniques unique to evaporative or electroplated bump technology. (Higgins, col. 3, Lines 52-57)

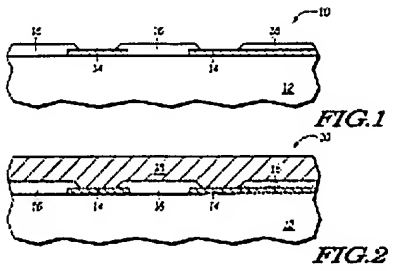


FIG.1

FIG.2

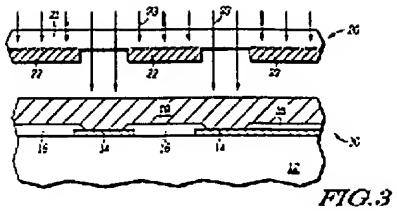


FIG.3

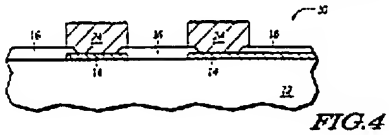


FIG.4

Regarding claim 12, Murphy et al. in view of Higgings teach the method in claim 11, wherein said passive devices comprise RF devices.

Murphy, (Col. 4, lines 10-15) teaches the method of forming capacitors, resistors, an inductors out of conductive polymer. It is known in the art that RF circuits comprise capacitors, inductors, and resistors. Capacitors, inductors, and resistors are passive devices, therefore it is obvious that passive devices comprise RF devices.

Regarding claim 13, Murphy et al. in view of Higgings teach the method in claim 11, wherein said passive devices comprise at least one of resistors, capacitors, and inductors. (Col. 4, lines 10-15)

Regarding claim 21, Murphy teaches a method of manufacturing an integrated circuit chip structure comprising:

supplying an integrated circuit chip; and

patterning a conductive polymer directly on an exterior conductor level of said integrated circuit chip, wherein said patterning produces passive devices.

(Murphy, Col. 4, lines 10-15)

Wherein said patterning is performed such that said passive devices comprise an integral part of said integrated chip. (holds no patentable weight – fails to further limit the scope from that of claim 11, the limitations and scopes of claims 11 and 21 are identical)

Murphy et al. teaches that the patterned passive devices are formed on the surface of a substrate. It is generally understood in the art, that an integrated circuit can be preformed on or in the substrate or produced after passive devices are formed. However, Murphy et al. does not explicitly teach that the conductive polymer film is formed on a supplied integrated circuit chip.

Higgins teaches the method in which an IC chip is provided (Higgins, Fig. 1 – IC Figs. 2-4 show patterning of conductive polymer layer 18). (Higgins, claims 1 & 14)

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to pattern a conductive polymer layer on a provided IC chip.

The application of the conductive polymer to the wafer and the subsequent lithographic processing involves straight forward processing technologies, without need for knowledge of the elaborate techniques unique to evaporative or electroplated bump technology. (Higgins, col. 3, Lines 52-57)

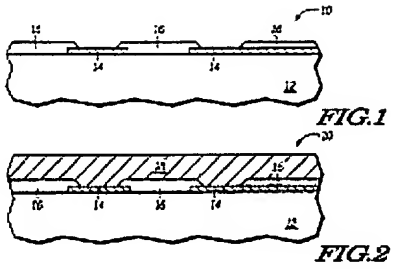


FIG.1

FIG.2

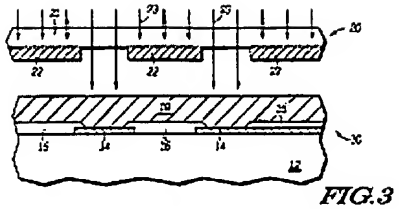


FIG.3

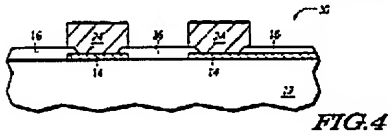


FIG.4

Regarding claim 22, Murphy et al. in view of Higgings teach the method in claim 11, wherein said passive devices comprise RF devices.

Murphy, (Col. 4, lines 10-15) teaches the method of forming capacitors, resistors, an inductors out of conductive polymer. It is known in the art that RF circuits comprise capacitors, inductors, and resistors. Capacitors, inductors, and resistors are passive devices, therefore it is obvious that passive devices comprise RF devices.

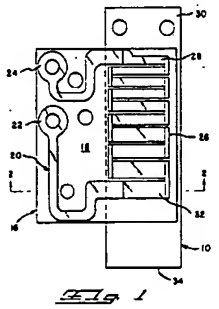
Regarding claim 23, Murphy et al. in view of Higgings teach the method in claim 21, wherein said passive devices comprise at least one of resistors, capacitors, and inductors. (Col. 4, lines 10-15)

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al. in view of Higgings in further view of Hansen et al. (US 4,115,750).

Regarding claim 14 & 24, Murphy et al. in view of Higgings teach the method in claim 13,

Murphy et al. in view of Higgings do not teach wherein said resistors comprise serpentine resistors.

Hansen et al. teaches the use of serpentine shape for a thin film resistor. (Hansen, Fig. 1 & Abstract)



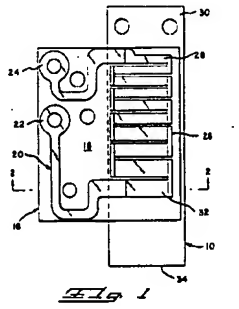
Therefore it would be obvious to one of ordinary skill in the art to use a serpentine shape when forming a thin film resistor.

> *A thin film resistor is fixed to the high expansion side of a bimetal element and, when energized, generates sufficient heat to actuate the bimetal. The resistor has a serpentine configuration formed by a continuous series of loops, each successive loop having a greater width from the fixed to the free end of the bimetal, to provide differential heating of the bimetal and thus a greater movement of its free end for the power dissipated in the resistor. (Hansen, Abstract)*

Regarding claim 24, Murphy et al. in view of Higgings teach the method in claim 23,

Murphy et al. in view of Higgings do not teach wherein said resistors comprise serpentine resistors.

Hansen et al. teaches the use of serpentine shape for a thin film resistor. (Hansen, Fig. 1 & Abstract)



Therefore it would be obvious to one of ordinary skill in the art to use a serpentine shape when forming a thin film resistor.

> *A thin film resistor is fixed to the high expansion side of a bimetal element and, when energized, generates sufficient heat to actuate the bimetal. The resistor has a serpentine configuration formed by a continuous series of loops, each successive loop having a greater width from the fixed to the free end of the bimetal, to provide differential heating of the bimetal and thus a greater movement of its free end for the power dissipated in the resistor. (Hansen, Abstract)*

Claim 15 & 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy et al. in view of Higgings in further view of Yoder (US 4,409,608).

Regarding claim 15, Murphy et al. in view of Higgings teach the method in claim 13.

Murphy et al. in view of Higgings do not teach wherein said capacitors comprise interdigitated capacitors.

Yoder teaches the method of forming a interdigitate shaped capacitor. (Yoder, col. 3, lines 10-18 & Fig. 4)

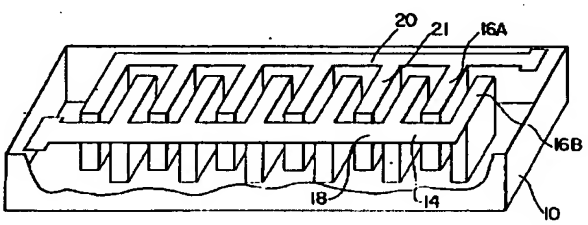


FIG. 4

It also is notoriously well known in the art to use a interdigitated design. Capacitance is given by C= εA/d, where ε is the permittivity, A is surface area, and d is the separation between surface area. From this well know equation, it is obvious that the can be controlled by the amount of surface area between two charge plates. It is know in the art to use this interdigitated design to increase and control capacitance while conserving space on the chip.

Therefore it would be obvious to one of ordinary skill in the art to form a interdigitated capacitor.

> *Alternate ones of the electrodes are interconnected forming the interdigitated plates of the capacitor with the dielectric comprising the insulating substrate material. The capacitor thus formed provides a high value of capacity with reduced chip area and both of the capacitor plates can be connected to other electronic components as desired including other electronic components disposed or embedded on the same substrate.* (Yoder, col. 3, lines 10-18)

Regarding claim 25, Murphy et al. in view of Higgings teach the method in claim 13.

Murphy et al. in view of Higgings do not teach wherein said capacitors comprise interdigitated capacitors.

Yoder teaches the method of forming a interdigitate shaped capacitor. (Yoder, col. 3, lines 10-18 & Fig. 4)

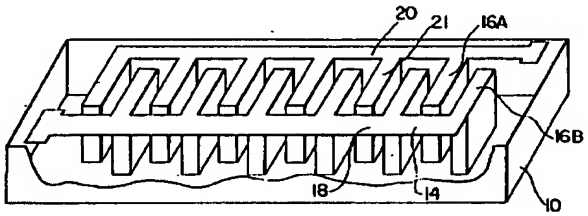


FIG. 4

It also is notoriously well known in the art to use a interdigitated design. Capacitance is given by $C = \varepsilon A/d$, where ε is the permittivity, A is surface area, and d is the separation between surface area. From this well know equation, it is obvious that

the can be controlled by the amount of surface area between two charge plates. It is know in the art to use this interdigitated design to increase and control capacitance while conserving space on the chip.

Therefore it would be obvious to one of ordinary skill in the art to form a interdigitated capacitor.

Alternate ones of the electrodes are interconnected forming the interdigitated plates of the capacitor with the dielectric comprising the insulating substrate material. The capacitor thus formed provides a high value of capacity with reduced chip area and both of the capacitor plates can be connected to other electronic components as desired including other electronic components disposed or embedded on the same substrate. (Yoder, col. 3, lines 10-18)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
April 3, 2006S

W. DAVID COLEMAN
PRIMARY EXAMINER